What is Claimed is:

1. A data processing device, comprising:

a central processing unit (CPU) with an instruction register operable to hold an instruction, wherein the CPU is operable to process a data word in response to the instruction;

an index register connected to the CPU and operable to provide a first address in response to the instruction; and

address circuitry connected to the CPU and operable to form a memory address of the data word by selecting a first portion of the first address from the index register and combining the first portion of the first address with a first portion of an immediate field selected from the instruction, wherein the first portion of the immediate field has a first width and the first portion of the first address has a second width.

2. The data processing device of Claim 1, wherein the address circuitry is operable to form the memory address by concatenating the first portion of the immediate field as a most significant address portion with the first portion of the first address as a least significant address portion.

3. The data processing device of Claim 1, further comprising decoding circuitry connected to the address circuitry and operable to select a first value for the first width from a first range of values responsive to the instruction.

4. The data processing device of Claim 3, wherein the decoder circuitry is further operable to select a second value for the second width from a second range of values responsive to the instruction.

5. The data processing device of Claim 4, wherein the decoder circuitry is further operable to parse the immediate field to determine a bit position for a first toggled bit.

6. A method for forming an address for accessing a data word in a data processing device while executing an instruction, the method comprising:

placing an immediate value in an immediate field of the instruction prior to executing the instruction, wherein the immediate value includes a base value;

accessing an index register within the data processing device specified by the instruction to obtain an index value; and

combining the index value with the base value to form the address for accessing the data word.

7. The method of Claim 6, wherein the step of combining further comprises concatenating the index value with the base value so that the base value forms a most significant portion of the address and the index value forms a least significant portion of the address, whereby a plurality of tables having different base addresses can be accessed with a common index value .

8. The method of Claim 7, wherein the step of combining further comprises decoding the immediate value to determine a width of the index value.

9. The method of Claim 8, wherein the step of decoding further comprises parsing the immediate value to determine a bit position for a first toggled bit and selecting the width of the index value in response to the bit position.

10. A method for accessing multiple data structures in a data processing system using a common index value, the method comprising:

fetching instructions for execution from an instruction memory of the data processing system;

initializing an index register within the data processing system with the common index value;

executing a first instruction having an indexed immediate addressing mode, wherein the first instruction has an immediate value comprising a first base value, such that a first data structure in a first portion of memory of the data processing system is accessed by the first instruction;

executing a second instruction having an indexed immediate addressing mode, wherein the second instruction has an immediate value comprising a second base value, such that a second data structure in a second portion of memory of the data processing system is accessed by the second instruction;

wherein the step of executing the first instruction further comprises:

accessing the index register within the data processing system specified by the first instruction to obtain the common index value; and

combining the common index value with the first base value to form an address for accessing the first data structure; and

wherein the step of executing the second instruction further comprises:

accessing the index register within the data processing system specified by the second instruction to obtain the common index value; and

combining the common index value with the second base value to form an address for accessing the second data structure, whereby the same common index value is used to access multiple data structures in the data processing system.

11. A method for performing multi-way branching in a data processing system, the method comprising:

fetching instructions in an ordered sequence for execution from an instruction memory of the data processing system;

reading a data value indicative of a target address from a first portion of memory of the data processing system;

initializing an index register within the data processing system with the data value;

executing a branch instruction having an indexed immediate addressing mode, wherein the branch instruction has an immediate value comprising a first base value, such that the ordered sequence for execution includes an instruction located in the instruction memory at an address specified by a combination of the first base value and the data value;

wherein the step of executing the branch instruction further comprises:

accessing the index register within the data processing system specified by the branch instruction to obtain the data value; and

combining the data value with the first base value to form an address for branching to.

12. A method for performing multi-way branching in a data processing system, the method comprising:

forming a branch table in a first portion of memory of the data processing system;

fetching instructions in an ordered sequence for execution from an instruction memory of the data processing system;

reading a data value indicative of a target address from a second portion of memory of the data processing system;

initializing an index register within the data processing system with the data value;

executing a branch instruction having an indexed immediate addressing mode, wherein the branch instruction has an immediate value comprising a first base value which points to the branch table, such that the

ordered sequence for execution includes an instruction located in the instruction memory at an address specified by an entry in the branch table indicated by the data value;

wherein the step of executing the branch instruction further comprises:

accessing the index register within the data processing system specified by the branch instruction to obtain the data value;

combining the data value with the first base value to form an address of an entry in the branch table; and

branching to an instruction at an address specified by the entry in the branch table.

13. An audio reproduction system, comprising:

means for acquiring a stream of data which contains encoded audio data;

a data device for processing the stream of data connected to the means for acquiring, the data device operable to form at least one channel of PCM data on an at least one device output terminal;

a digital to analog converter connected to the output terminal operable to convert the channel of PCM data to an analog audio signal on a D/A output terminal;

a speaker subsystem connected to the D/A output terminal; and

wherein the data device further comprises:

an instruction register operable to hold an instruction during processing by the data processing device;

a central processing unit (CPU) operationally connected to the instruction register and operable to process a data word in response to the instruction;

an index register operationally connected to the instruction register and operable to provide a first address in response to the instruction; and

address circuitry operable to form a memory address of the data word by selecting a first portion of the first address from the index register and combining the first portion of the first address with a first portion of an immediate field selected from the instruction, wherein the first portion of the immediate field has a first width and the first portion of the first address has a second width.

14. The audio reproduction system of Claim 13, wherein the means for acquiring comprises a satellite broadcast receiver.

15. The audio reproduction system of Claim 13, wherein the means for acquiring comprises a digital disk player.

16. The audio reproduction system of Claim 13, wherein the means for acquiring comprises a cable TV receiver.